CLAIMS

What is claimed is:

1. A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at lease one component including a polysilicon layer having a top surface;

a silicide on the top surface of the polysilicon layer of the at least one component;

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and

a conductor for filling the plurality of contact holes.

2. The flash memory device of claim 1 wherein the silicide further includes a titanium silicide.

3. The flash memory device of claim 1 wherein the silicide further includes a cobalt silicide.

4. The flash memory device of claim 1 wherein the component further include an oxide-nitride-oxide layer on the polysilicon layer and wherein the oxide-nitride-oxide

layer is removed prior to formation of the silicide.

5. The flash memory device of claim 4 wherein the oxide-nitride-oxide layer is removed during a second polysilicon layer etching step which forms the plurality of gate stacks.

6. The flash memory device of claim 4 wherein the plurality of gate stacks further include a plurality of spacers and wherein the oxide-nitride-oxide layer is removed after formation of the plurality of spacers.

7. The flash memory device of claim 1 further comprising:

at least one field oxide region, the at least one component being located on the at least one field oxide region.

8. A method for providing at least one contact in a flash memory device, the flash memory device including a plurality of gate stacks and at lease one component including a polysilicon layer having a top surface, the method comprising the steps of:

(a) forming a silicide on the top surface of the polysilicon layer;

(b) providing an insulating layer covering the plurality of gate stacks, the at least one component and the silicide;

(c) etching the insulating layer to provide at least one contact hole, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer;

(d) filling the at least one contact hole with a conductor.

9. The method of claim 8 wherein the at least one contact hole further includes a plurality of contact holes, wherein a plurality of source/drain regions are adjacent to the plurality of gate stacks, and wherein the insulating layer etching step (c) further includes the steps of:

(c1) etching the insulating layer to expose a portion of the plurality of gate stacks in a first portion of the plurality of contact holes, to expose a portion of the plurality of source/drain regions in a second portion of the plurality of contact holes and to expose the silicide on the at least one polysilicon device in a third portion of the plurality of contact holes.

10. The method of claim 8 wherein the silicide further includes a titanium silicide.

11. The method of claim 8 wherein the silicide further includes a cobalt silicide.

12. The method of claim 8 wherein the component further include an oxide-nitride-oxide layer on the polysilicon layer and wherein the method further includes the step of:

(e) removing the oxide-nitride-oxide layer prior to formation of the silicide.

13. The method of claim 12 wherein the oxide-nitride-oxide layer removing step

(e) further includes the step of:

(e1) removing the oxide-nitride-oxide layer during a polysilicon layer etching step which forms the plurality of gate stacks.

14. The method of claim 12 wherein the plurality of gate stacks further include a plurality of spacers and wherein the oxide-nitride-oxide layer removing step (e) further includes the step of:

(e1) removing the oxide-nitride-oxide layer after formation of the plurality of spacers.

15. The method of claim 8 wherein the flash memory device further includes at least one field oxide region, the at least one component being located on the at least one field oxide region.

16. The method of claim 8 wherein the silicide forming step (a) further includes the step of:

(a1) using a self-aligned silicide process to form the silicide on the top surface of the polysilicon layer.